REMARKS

Applicant has reviewed and considered the Office Action mailed on July 8, 2005, and the references cited therewith.

Claims 18, 20, and 21 are amended, no claim are canceled, and claims 31-34 are added; as a result, claims 1, 4-8, 10-13, 15-23, 25-29, and 31-34 are now pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Supplemental Information Disclosure Statement filed on April 20, 2005, marked as being considered and initialed by the Examiner, be returned with the next official communication.

§102 Rejection of the Claims

Claims 4-7, 18, 19 and 26 were rejected under 35 USC § 102(b) as being anticipated by Webb (U.S. Patent No. 4,855,625). Applicant respectfully traverses this rejection with respect to claims 4-7 and 26.

The office action alleges that Q3 of Webb "can be read as a bias circuit which is capable of increasing collector-to-emitter bias current in the input transistor (Q1)". Applicant respectfully disagrees. According to the disclosure of Webb, the addition of Q3 (and placing it in the same dielectrically isolated island as Q1 and Q2) decreases the current in the input transistor rather than increasing the bias current as alleged in the office action. For example, at column 4, lines 14-20, Webb states that "[b]y incorporating the bias transistor Q3 into the same dielectrically isolated island with transistors Q1 and Q2 ... the ratio of the collector currents in transistors Q1 and Q2 can be increased to a value on the order of 1:50, nearly an order of magnitude improvement over the prior art." The increase in the ratio of collector currents is achieved by ***reducing*** the current in the input transistor. As described by Webb at column 4, lines 4-8, "[b]y elimination of the parasitic capacitance, the collector current of the input transistor Q1 of the Darlington pair can be ***reduced*** significantly relative to the collector current of transistor Q2." [Emphasis added].

Applicant respectfully submits that Webb does not disclose, teach or suggest "a bias circuit to increase a collector-to-emitter bias current in the input transistor" as recited in claim 4. Further, applicant respectfully submits that Webb does not disclose, teach, or suggest "increasing a bias current in an input transistor of a Darlington pair by providing a current path from, and a voltage path to, an emitter of the input transistor" as recited in claim 26. Accordingly, claims 4 and 26 are believed to be in condition for allowance, and applicant respectfully requests that the rejection of independent claims 4 and 26 be withdrawn. In addition, claims 5-7 are believed to be in condition for allowance at least by virtue of dependency on claim 4, and applicant respectfully requests that the rejection of claims 5-7 be withdrawn.

Independent claim 18 has been amended to recite an increase in a collector-to-emitter bias current in the input transistor of the Darlington pair. As described above regarding claims 4 and 26, applicant respectfully submits that Webb does not disclose an increase in collector-to-emitter bias current. Accordingly, applicant respectfully submits that the amendment to claim 18 has overcome the rejection under 35 USC § 102(b), and requests that the rejection be withdrawn. Claim 19 is believed to be in condition for allowance at least by virtue of dependency on claim 18, and applicant respectfully requests that the rejection of claim 19 be withdrawn.

§103 Rejection of the Claims

Claims 1, 12, 15, 22 and 23 were rejected under 35 USC § 103(a) as being unpatentable over Leung (U.S. Patent No. 5,548,288). Applicant respectfully traverses this rejection. In support of this rejection, the office action states that "Leung (Fig. 3) discloses an input transistor (MN1) and a second transistor (MN2) coupled as a Darlington pair". Applicant respectfully disagrees. A Darlington pair "is a composite two-transistor device in which the collectors are tied together and the emitter of the first device drives the base of the second." See Paul R. Gray & Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 2nd Edition, pgs 190-191; a copy of which is being provided with this response. Consistent with Gray & Meyer, the instant application defines a Darlington pair on page 2, lines 10-12 as follows:

> Input transistor 110 and second transistor 120 are coupled to form a Darlington transistor pair with the collectors coupled

together at node 142, and the emitter of input transistor 110 coupled to the base of transistor 120 at node 111.

Applicant respectfully submits that Leung does not include two transistors having collectors (or drains, in the case of MOS transistors) coupled together to form a Darlington pair. The drain of MN1 is coupled to a voltage V+, and the drain of MN2 is coupled either to a current source Iref or to an output node Out. Therefore, MN1 and MN2 of Leung are not coupled as a Darlington pair as alleged in the office action.

Accordingly, applicant respectfully submits that a *prima facie* case of obviousness has not been presented, and respectfully requests the withdrawal of the rejection of claims 1, 12, 15, 22 and 23 under 35 USC § 103(a) as being unpatentable over Leung.

Claim 8 is rejected under 35 USC § 103(a) as being unpatentable over Webb (U.S. Patent No. 4,855,625). This rejection relies on the rejection of claim 4 under 35 USC § 102(b) as discussed above. The rejection of claim 4 has been traversed, and applicant respectfully believes that claim 4 is in condition for allowance. For the same reasons presented above with regard to claim 4, applicant respectfully believes that a *prima facie* case of obviousness has not been presented with regard to claim 8, and respectfully requests that the rejection of claim 8 be withdrawn.

Allowable Subject Matter

Claims 10, 11, 13, 16, 17, 20, 21, 25, and 27-29 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10, 11, 13, 16, 17, 25, and 27-29 have not been amended, and applicant respectfully believes that these claims are in condition for allowance in their present form for the reasons explained in the remarks above. Claims 20 and 21 have been rewritten in independent form including all of the limitations of the base claim and any intervening claims.

New Claims

Claims 31-34 have been added. Claims 31 and 32 depend on claim 20 which has been found to be allowable. Claims 33 and 34 depend on claim 21 which has been found to be allowable. Claims 31-34 are believed to be in condition for allowance at least by virtue of dependency. No new matter has been added.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (952-473-8800) to facilitate prosecution of this application.

Respectfully submitted,

KEVIN W. GLASS ET AL.

By their Representatives,

Customer Number 45445
Telephone Number 952-473-8800

Date 10-10-05 By Dana B LeMoine
Dana B. LeMoine
Reg. No. 40,062

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 10 day of October, 2005.

Chris Hammond
Name

Chris Hammond
Signature

ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

SECOND EDITION

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ROBERT G. MEYER

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equivalent can be used to represent the performance of the composite device, thus simplifying the analysis of circuits containing composite transistors.

The Darlington configuration, illustrated in Fig. 3.21, is a composite two-transistor device in which the collectors are tied together and the emitter of the first device drives the base of the second. A biasing element of some sort is required to control the emitter current of Q_1. The result is a three-terminal composite transistor that can, in principle, be used in place of a single transistor in common-emitter, common-base, and in common-collector configurations. When used as an emitter follower, the device is identical to the CC–CC connection already discussed. When used as a common-emitter amplifier, the device is very similar to the CC–CE connection, except that the collector of Q_1 is connected to the output instead of to the power supply. The effect of this change is to reduce the effective output resistance of the device because of feedback through r_o of Q_1, and to cause the input capacitance to increase because of the connection of the collector-base capacitance of Q_1 from the input to the output. Because of these drawbacks, the CC–CE connection is normally preferable in integrated small-signal amplifiers. The term Darlington is often used to refer to both the CC–CE and CC–CC connections.

EXAMPLE

Find the effective r_π^c, β^c, and g_m^c for the composite transistor shown in Fig. 3.18. Assume, for both devices, that $\beta_0 = 100$, $r_b = 0$, and $r_o = \infty$. Assume for Q_2 that $I_C = 100\ \mu A$ and that $I_{bias} = 10\ \mu A$.

Solution:

The base current of Q_2 is $100\ \mu A/100 = 1\ \mu A$. Thus the emitter current of Q_1 is $11\ \mu A$.

$$r_{\pi 1} = \frac{\beta_0}{g_m} = \frac{100}{11\ \mu A/26\ mV} = 236\ k\Omega$$

$$g_{m1} = (2.36\ k\Omega)^{-1}$$

$$r_{\pi 2} = 26\ k\Omega$$

$$g_{m2} = (260\ \Omega)^{-1}$$

$$r_\pi^c = 236\ k\Omega + (101)(26\ k\Omega) = 2.8\ M\Omega$$

$$\beta^c = (101)(100) = 10{,}100$$

$$g_m^c = g_{m2}(0.916) = (283\ \Omega)^{-1}$$

Thus the composite transistor has much higher input resistance and current gain than a single transistor.

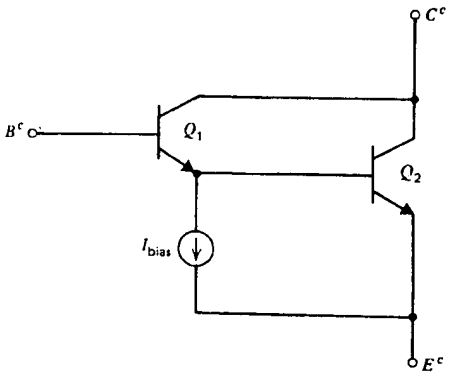

Figure 3.21 The Darlington configuration.

3.3.2 The CE – CB, or Cascode, Configuration

The cascode two-transistor subcircuit is shown in Fig. 3.22. The principal attributes of this configuration are that the output resistance is very high and that no high-frequency feedback occurs from the output back to the input through C_μ as occurs in the common-emitter configuration.[4] The high output impedance attainable is particularly useful in attaining power supply desensitization in bias reference supplies and achieving large amounts of voltage gain in a single amplifying stage with an active *pnp* load. These applications are discussed further in Chapter 4. In this section we calculate the low-frequency, small-signal properties of the CE–CB connection. We will assume that r_b in both devices is zero; in considering the high-frequency performance of this combination we must account for the effects of r_b on the frequency response as discussed in Chapter 7. The base resistances have a negligible effect on the low-frequency performance.

The small-signal equivalent circuit for the cascode circuit is shown in Fig. 3.23. Since we are considering only the low-frequency performance, we neglect the capacitive energy storage elements. We will determine the input resistance, output resistance, and transconductance of the cascode circuit. By inspection of Fig. 3.23, the input resistance is simply r_π of Q_1. Since the current gain from emitter to collector of Q_2 is nearly unity, the transconductance of the circuit from input to output is approximately equal to the transconductance of Q_1. The output resistance can be calculated by applying a test voltage source, v_x, to the collector of Q_2 and calculating the current, i_x, which results as shown in Fig. 3.24. We first note

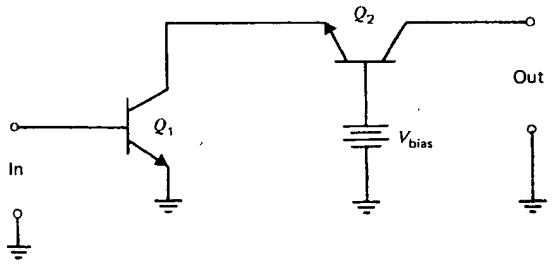

Figure 3.22 The cascode amplifier.